Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **CLR1**
2. **D1**
3. **PR1**
4. **Q1**
5. **N.Q1**
6. **GND**
7. **N.Q2**
8. **Q2**
9. **PR2**
10. **D2**
11. **CLR2**
12. **VCC**

**.042”**

**.042”**

**11**

**10**

**2 1 14 13 12**

**3**

**4**

**5 6 7 8 9**

**LS**

**74A**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si Ni**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: LS74A**

**APPROVED BY: DK DIE SIZE .042” X .042” DATE: 1/10/18**

**MFG: TEXAS INSTRUMENTS THICKNESS .014” P/N: 54LS74**

**DG 10.1.2**

#### Rev B, 7/19/02